National Taiwan University

How to use eGaN Correctly

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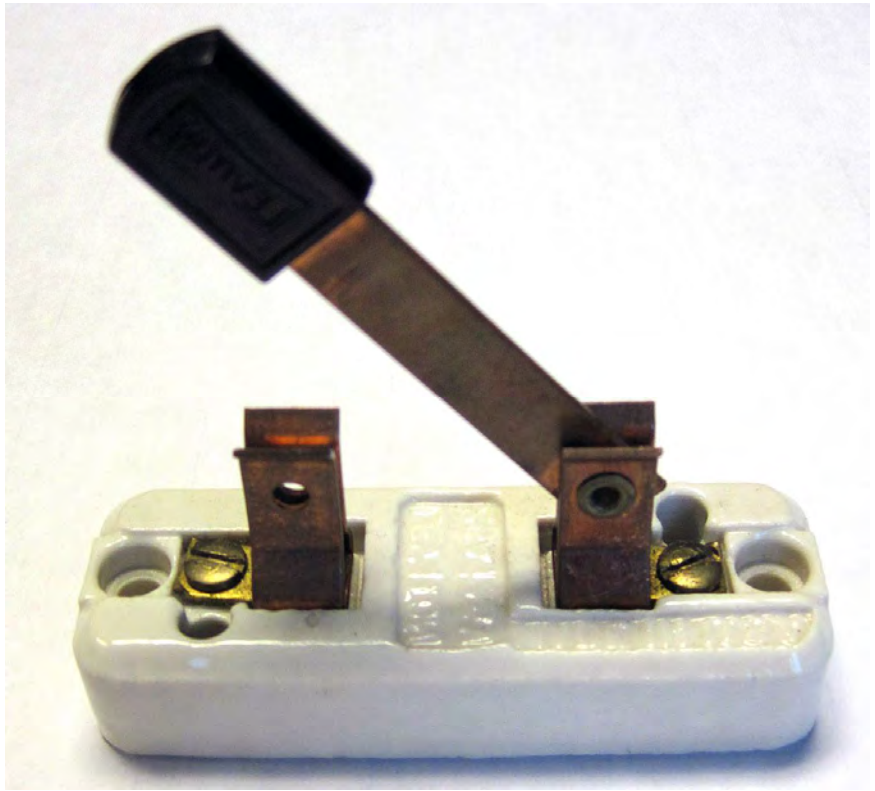
Agenda

- What is the Ideal Switcher?
- eGaN FETs Features & Benefits
- eGaN FETs Drivers
- Layout, Layout, Layout !
- Design Example

The Ideal Power Switch

- Block Infinite Voltage
- Carry Infinite Current
- Switch In Zero Time
- Zero Drive Power
- Normally Off



eGaN FETs
Key Features & Benefits

- Enhancement-Mode devices
- Rds(on) per unit area is much smaller
- Much faster switching (tr/tf) time
- Very low Qg and capacitance
- Provide much higher light load efficiency
- No parasitic PN junction body (Qrr=0)

eGaN Characteristics

Note:
All curves here use EPC2001 (100V, 7mΩ)

Figure 2: Transfer Characteristics

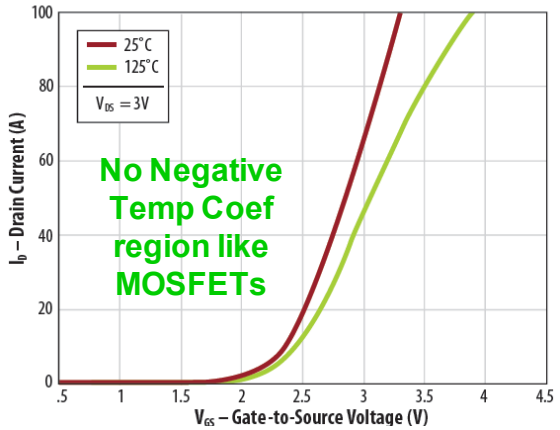


Figure 4: $R_{DS(on)}$ vs V_{GS} for Various Temperature

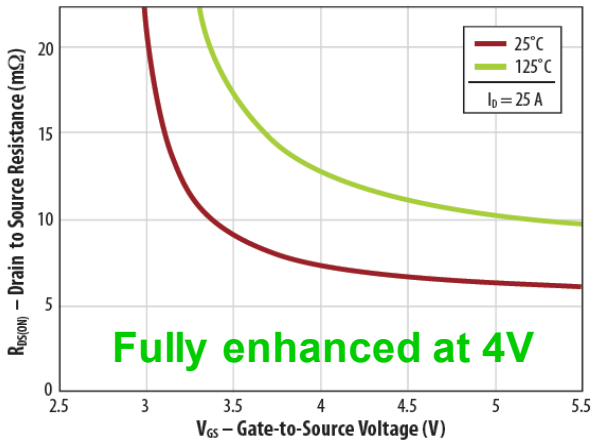


Figure 9: Normalized Threshold Voltage vs. Temperature

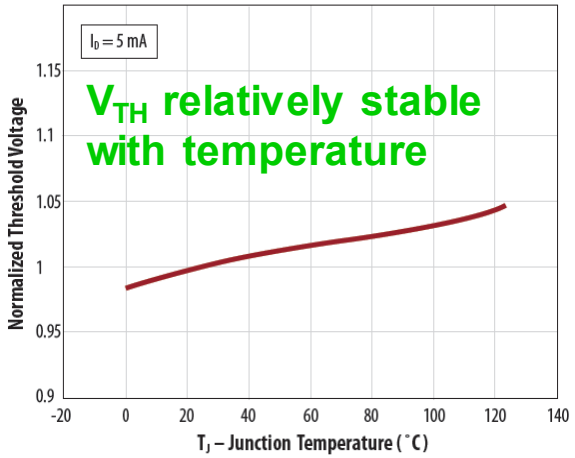


Figure 6: Gate Charge

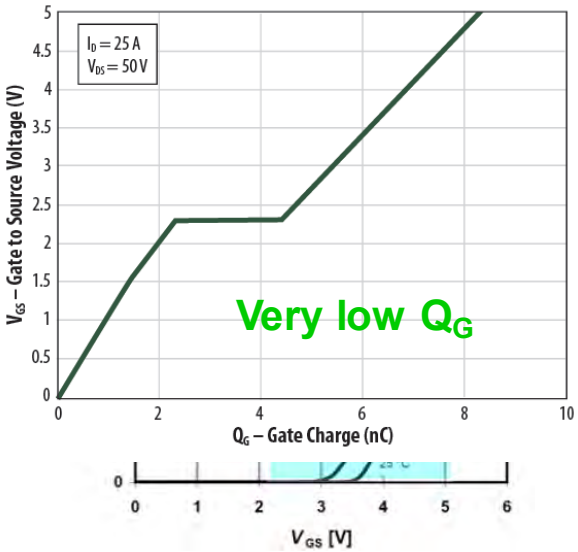
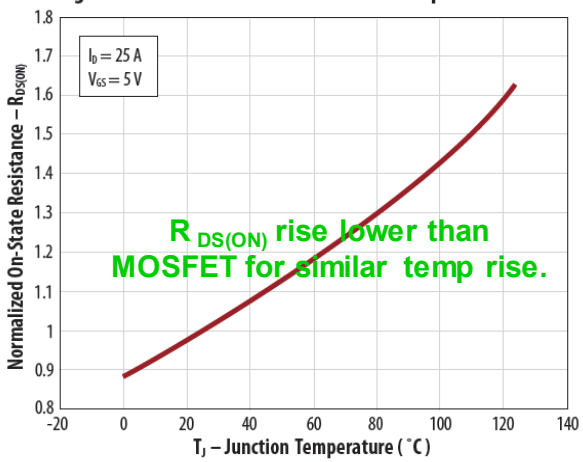
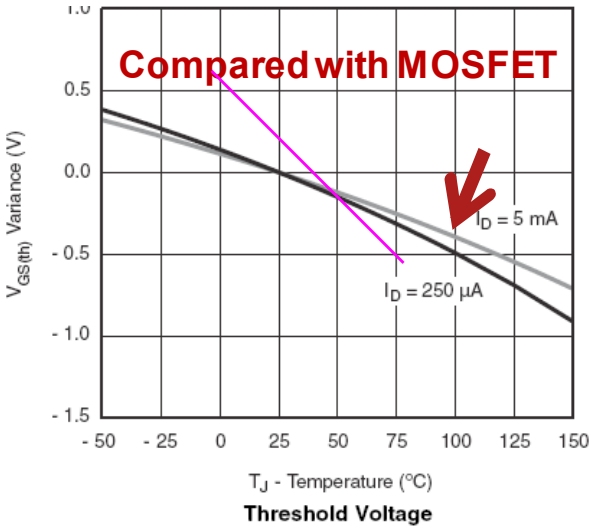
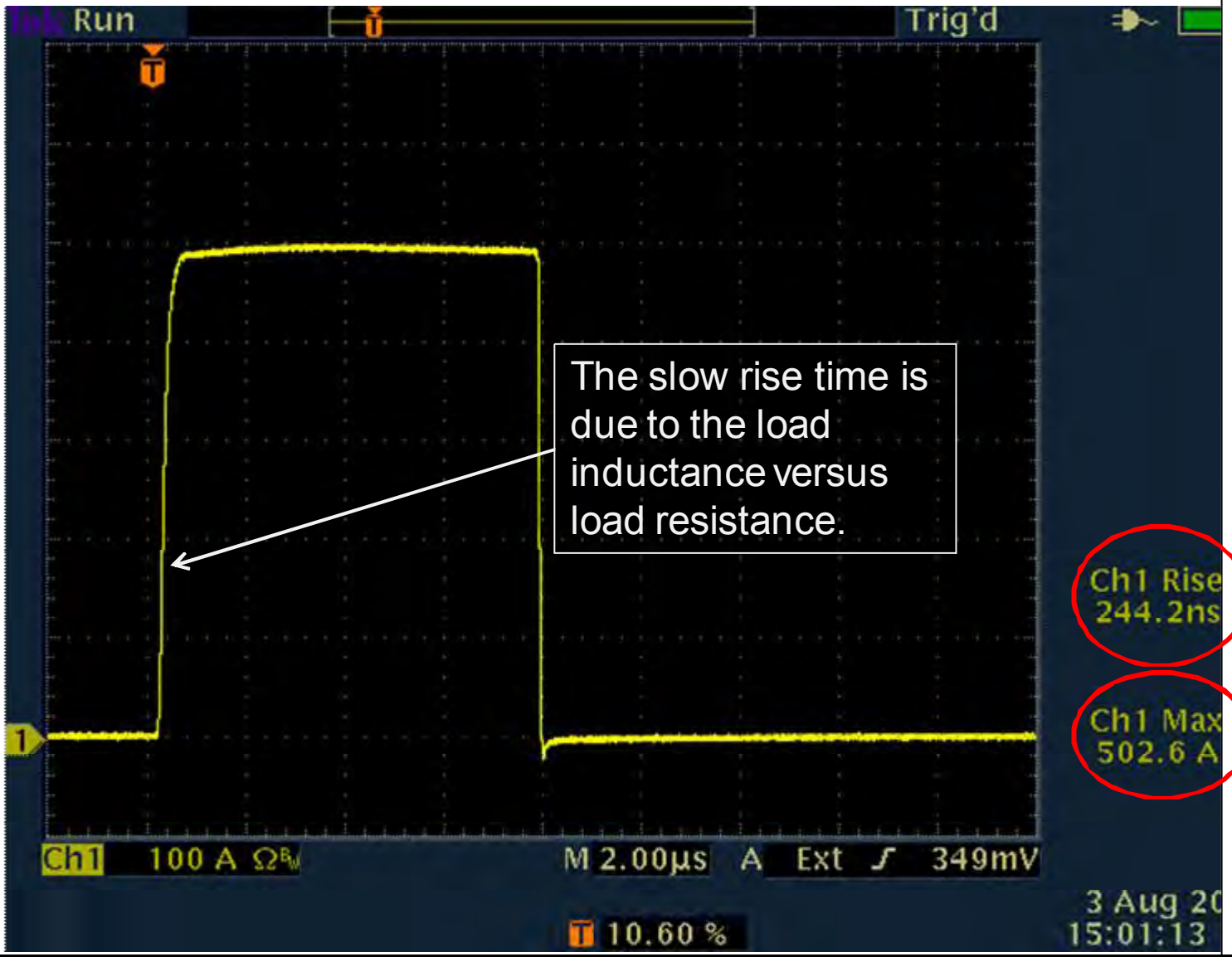


Figure 8: Normalized On Resistance Vs Temperature





8 * EPC2010 paralleling
500A, 10uS, 100Hz



eGaN® FETs are Easy to Use

It's just like a MOSFET

except for TWO things

(1)

The hyper high frequency capability makes circuits using eGaN® FET very sensitive to layout

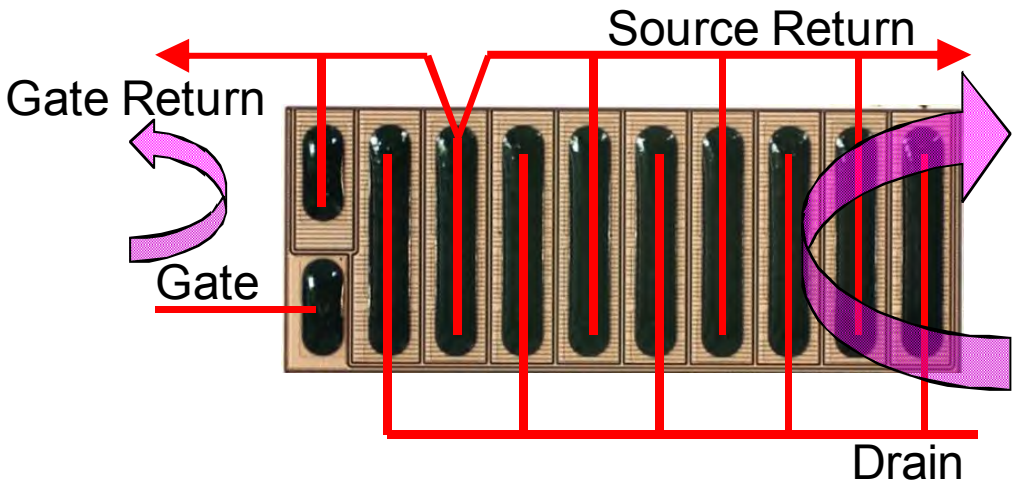
(2)

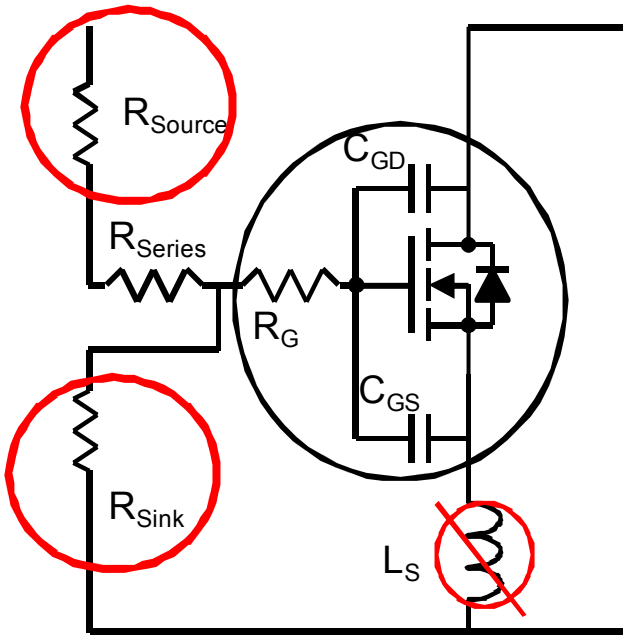
eGaN® FET are more sensitive to gate rupture than power MOSFETs

Gate Drive Constraints

- V_{GS} = 6V max, but **4.5V needed** to fully enhance
- High frequency layout required
  - switching time 2-5ns range
- Fast switching causes opportunity for false turn on. dv/dt immunity decreases as device voltage rating increases. A gate drive with a low resistance turn-off (pull-down) is needed.
- The diode V_f is higher than silicon and therefore the gate drive needs to help minimize diode conduction.
- Zero reverse recovery allows very short pulse widths

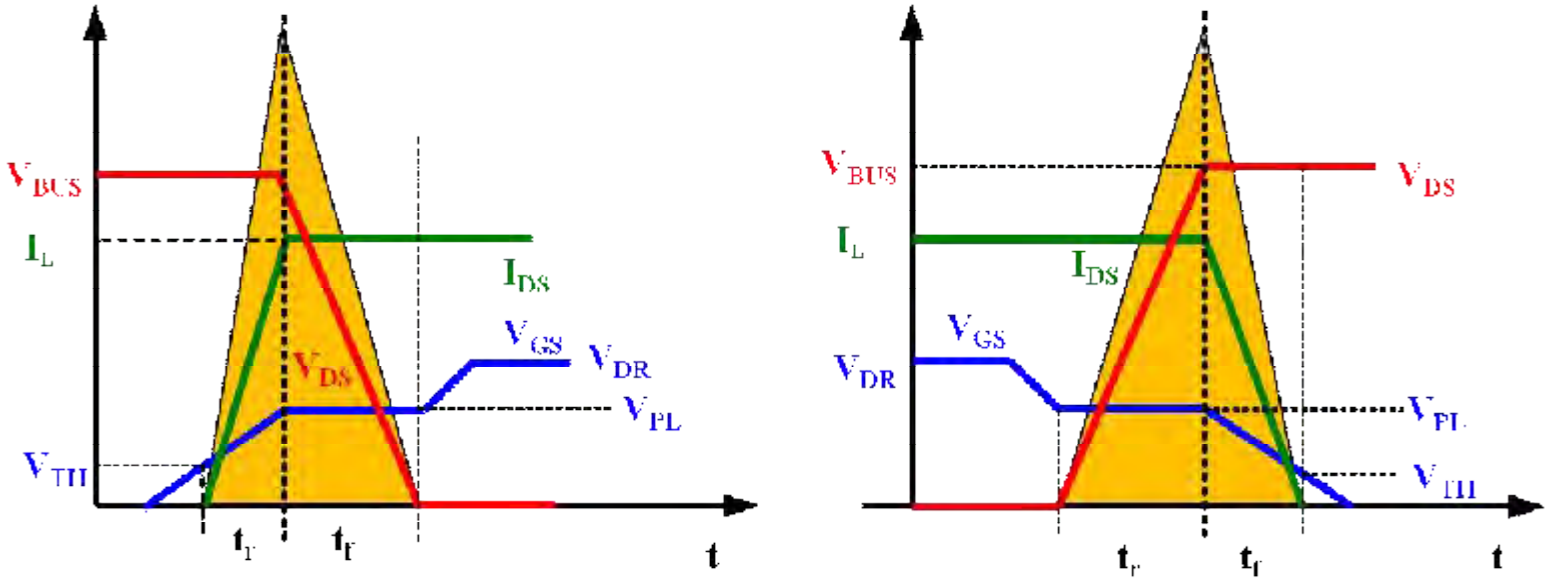
Layout





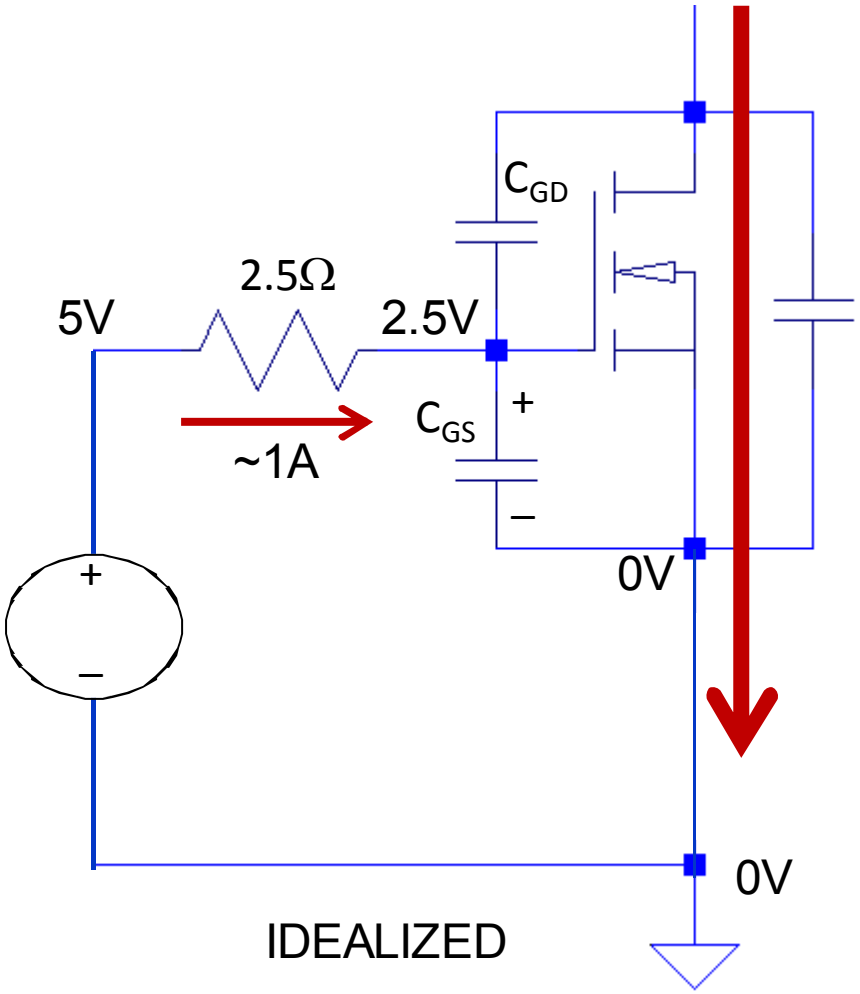
Minimize Common Source Inductance (CSI)

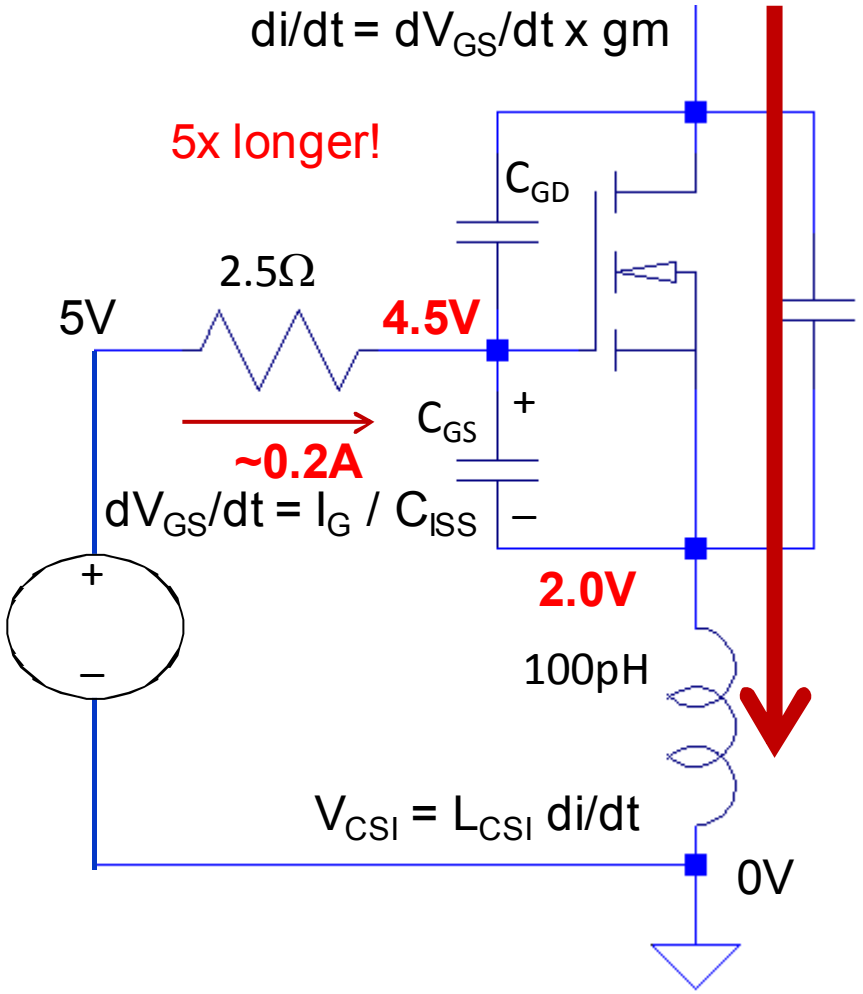
Switching Interval



- Assumes turn-on / off symmetrical
- Neglects RMS loss effect of C_{OSS} dv/dt current
- Neglects di/dt effect of C_{OSS} dv/dt current
- Neglects miller effect of di/dt across L_{loop}
- Neglects gate inductance

Effect on Common source inductance



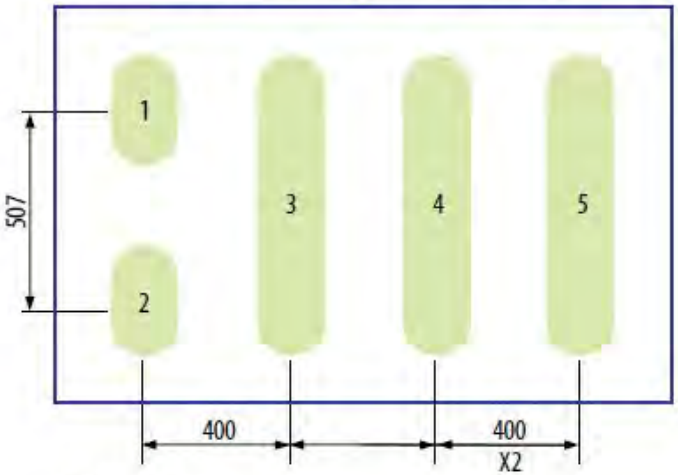


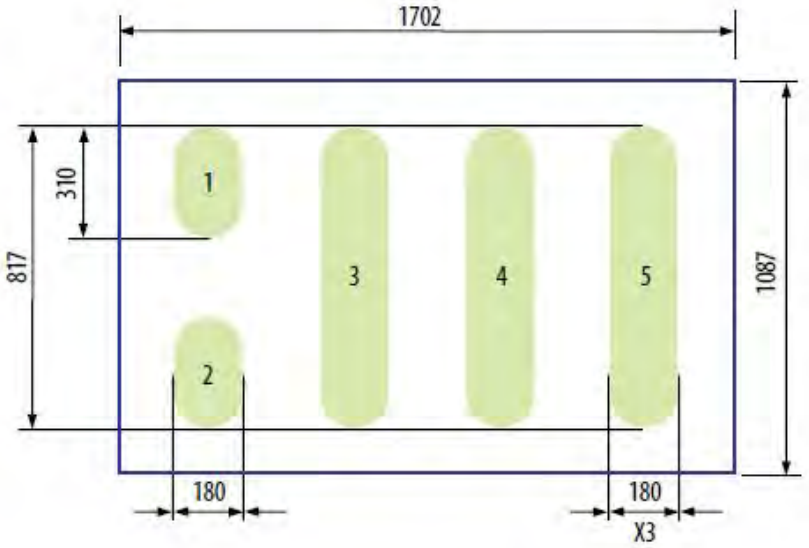
$$I_G \sim \Delta V / (L_{CSI} . g_M / C_{ISS} + R_G)$$

PCB Land Pattern

RECOMMENDED LAND PATTERN
(measurements in µm)

The land pattern is solder mask defined
Solder mask is 10um smaller per side than bump



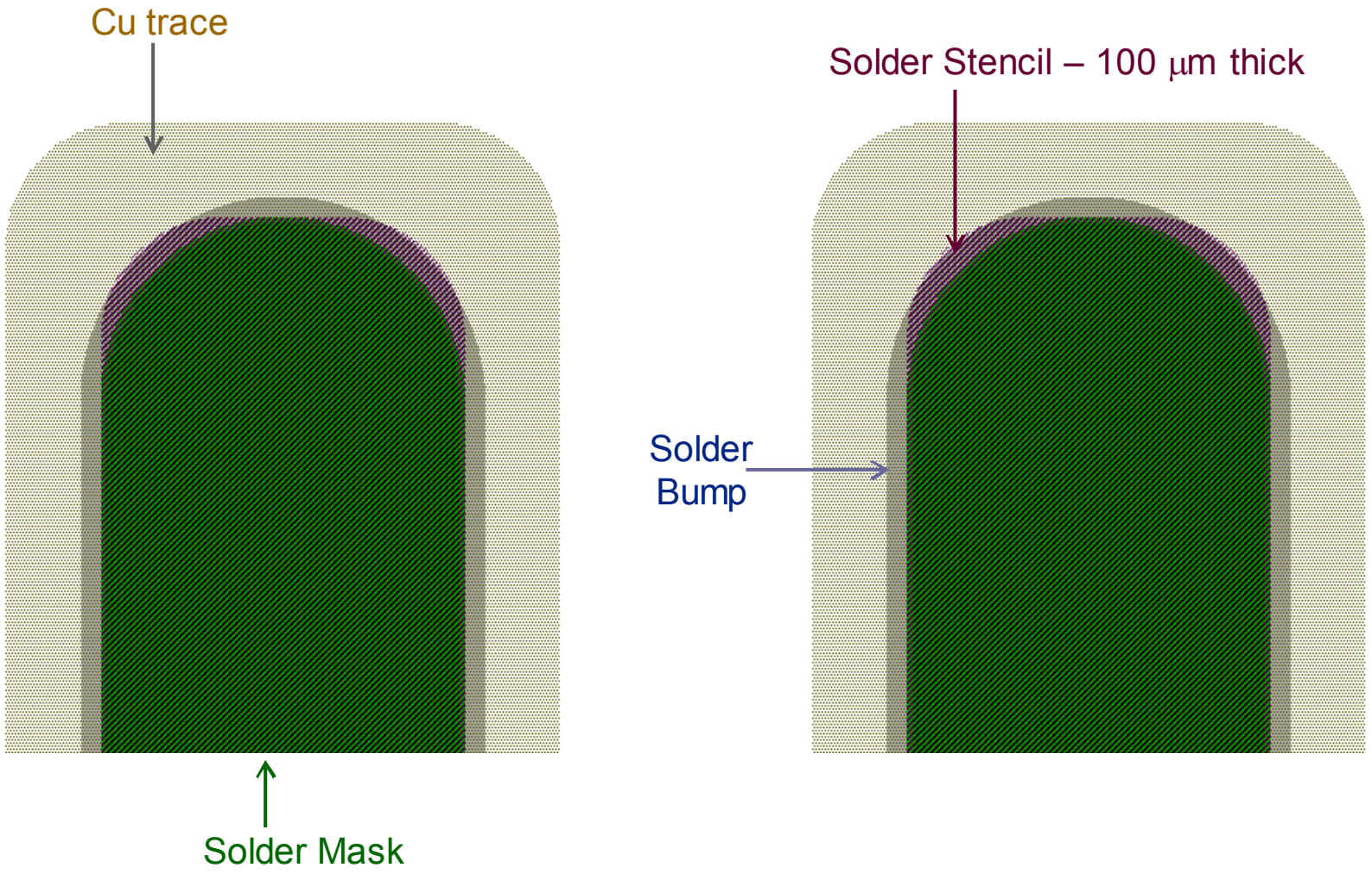


Pad no. 1 is Gate
Pad no. 2 is Substrate
Pad no. 3 and 5 are Drain
Pad no. 4 is Source

Recommended Land Pattern is Defined in the Datasheet

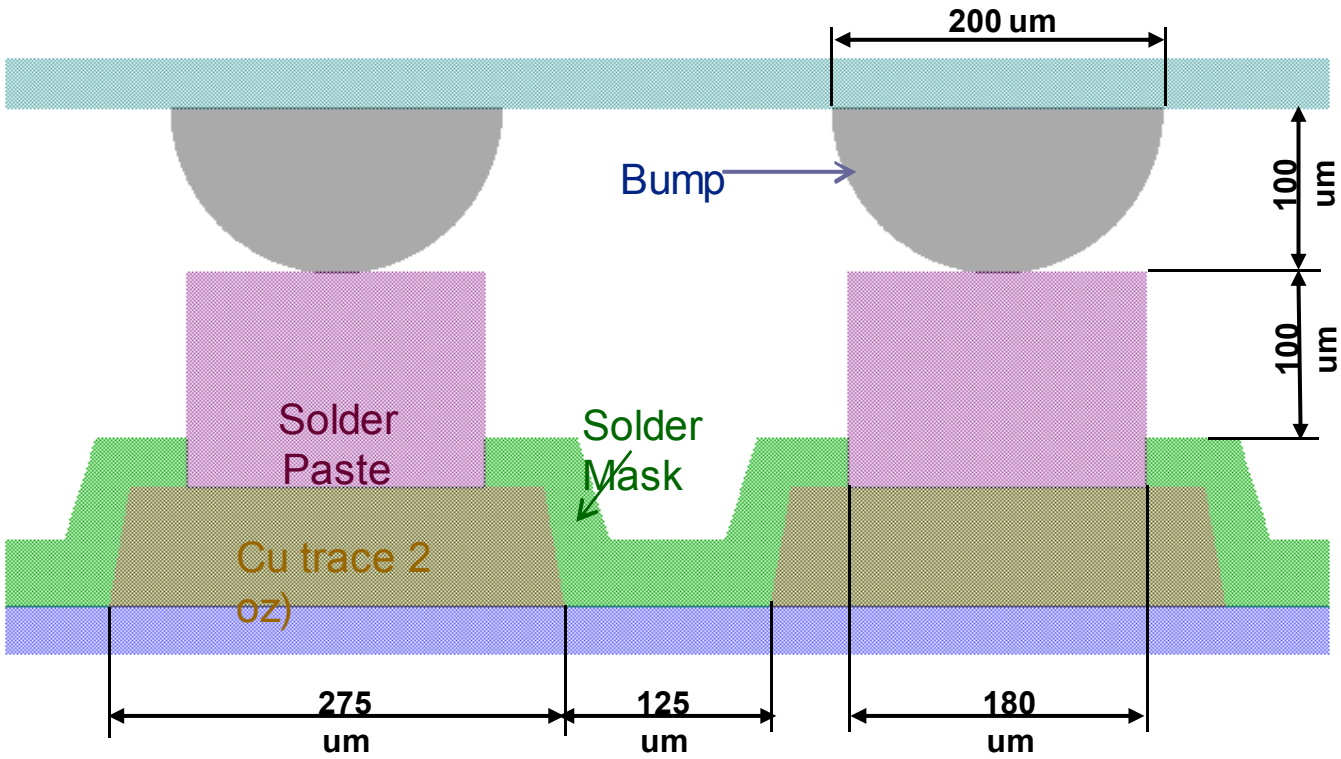
PCB Top View

Relative Sizes (Cu trace, Solder mask, Bump, Stencil)



PCB Cross Section

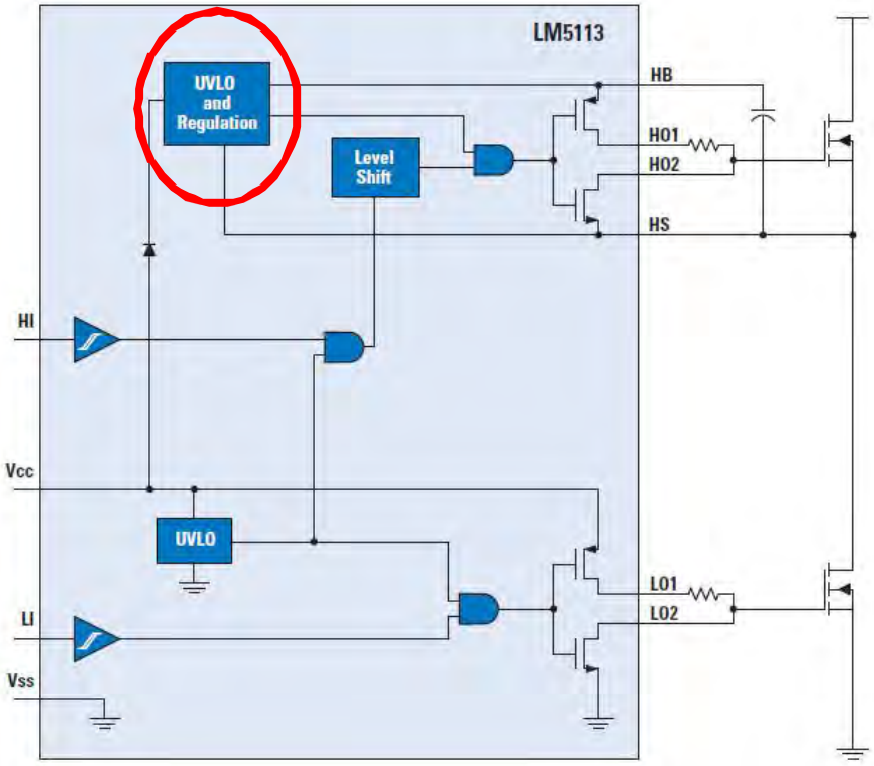
Relative Dimensions (Cu trace, solder mask, Bump, stencil)
EPC2001, EPC2007, EPC2014, EPC2015



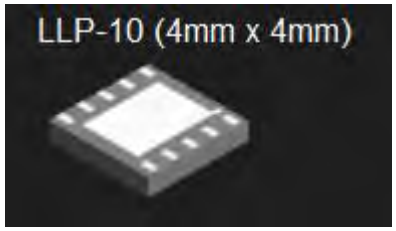
No Stencil Bench Mount - Tacky flux part number: Kester TSF-6502

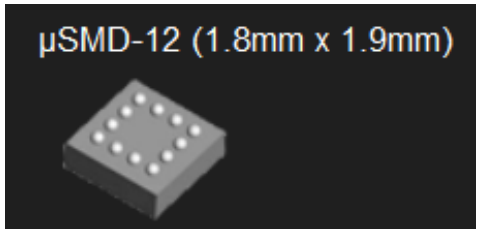
Drivers

LM5113

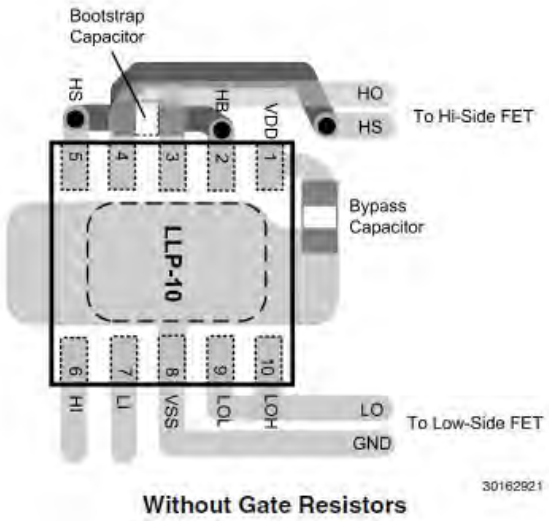


LM5113 bootstrap voltage regulation, synchronous buck converter evaluation board. Input 48V; output 10V; switching frequency at 800 KHz.

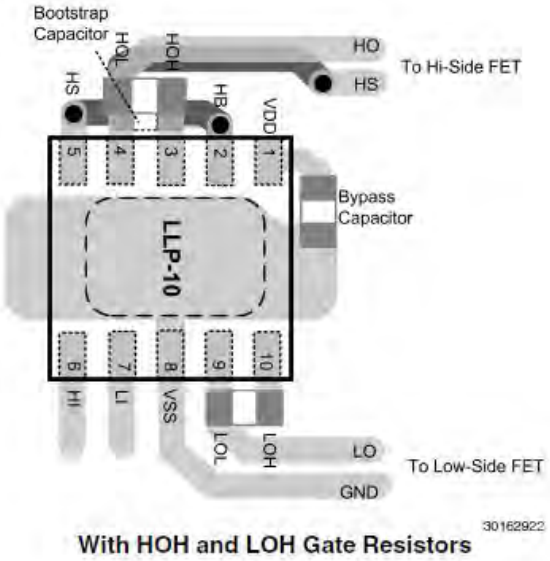




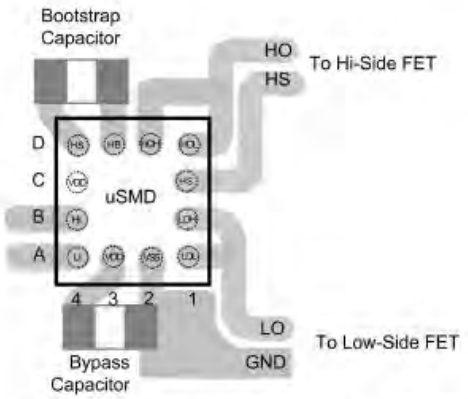
LM5113 layout reference



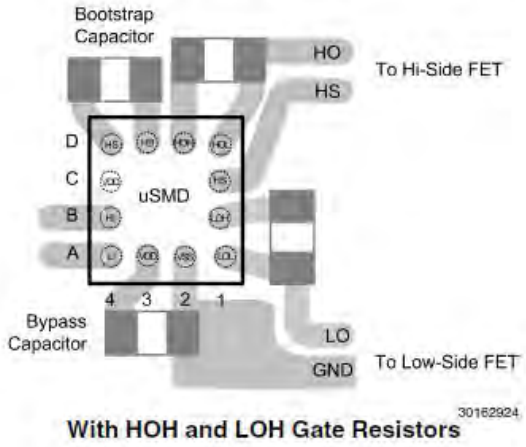
Without Gate Resistors



With HOH and LOH Gate Resistors



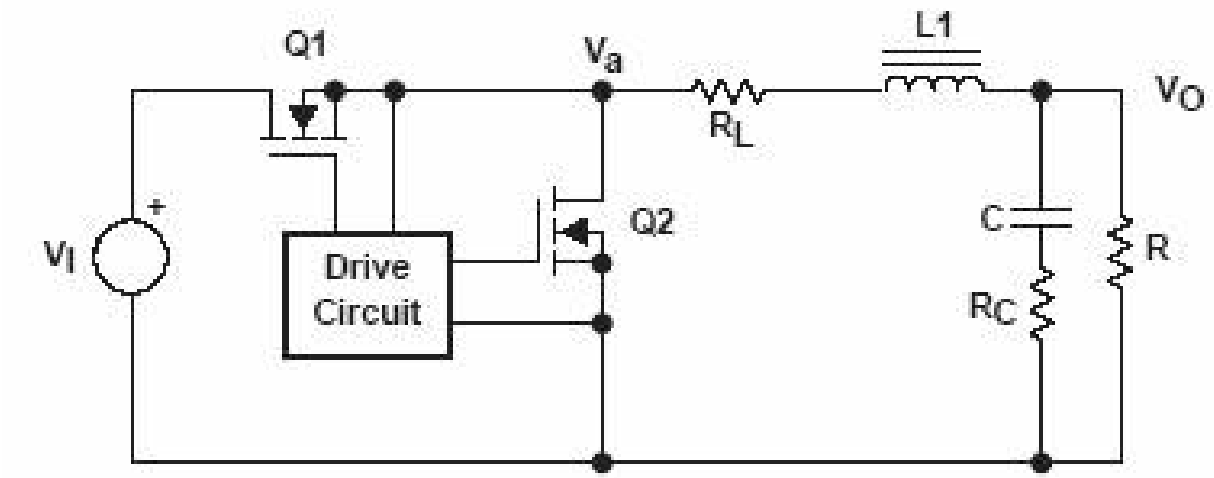
Without Gate Resistors

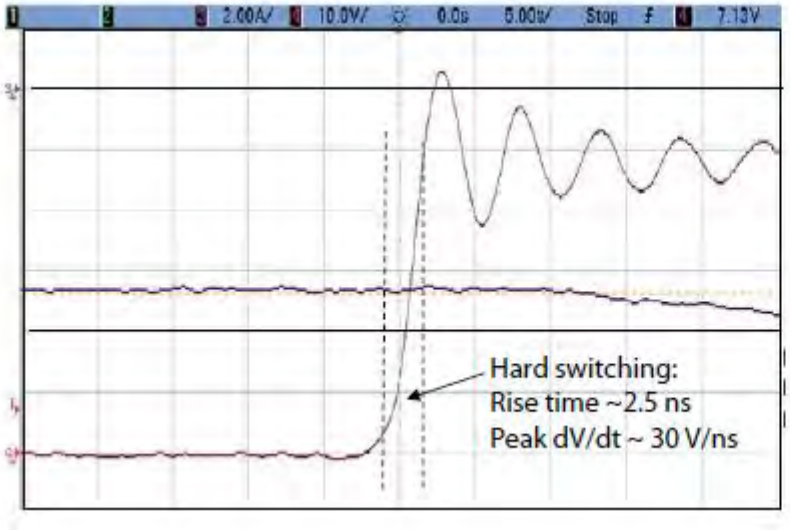


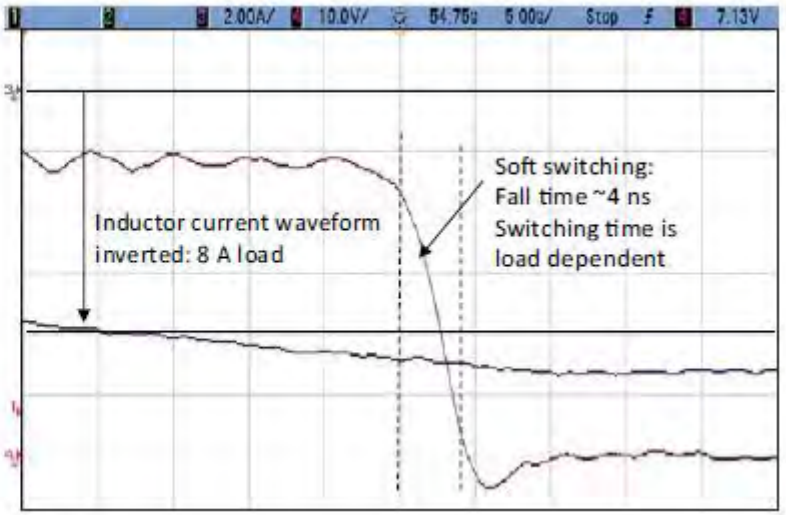
With HOH and LOH Gate Resistors

TI driver layout recommendation
4 external components placement !
Close to driver IC

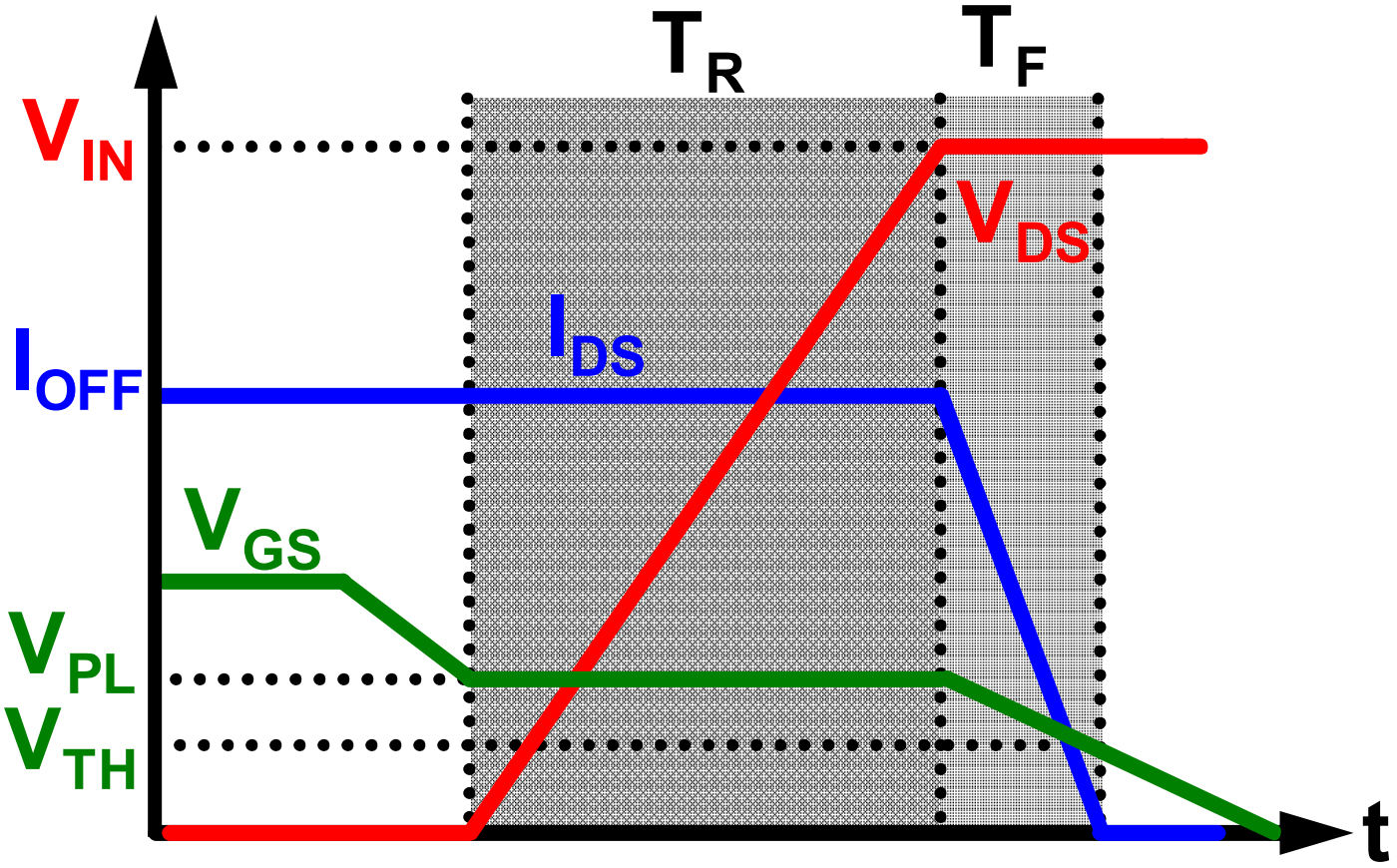
Example: Buck Converter







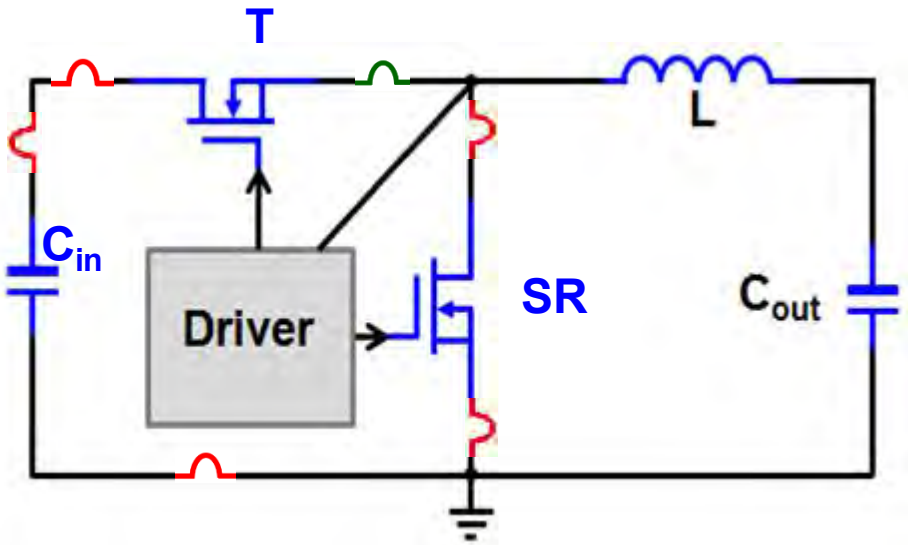
Ideal Hard Switching



$$P_{T_R} \approx \frac{V_{IN} * I_{OFF} * Q_{GD}}{2 * I_G}$$

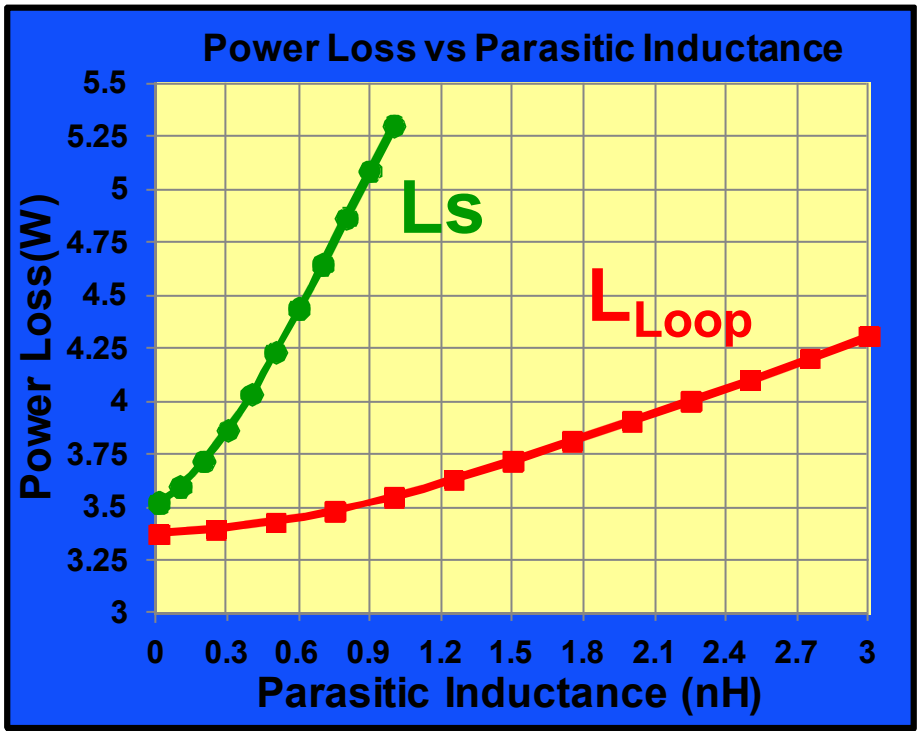
$$P_{T_F} \approx \frac{V_{IN} * I_{OFF} * Q_{GS2}}{2 * I_G}$$

Buck Converter Parasitics



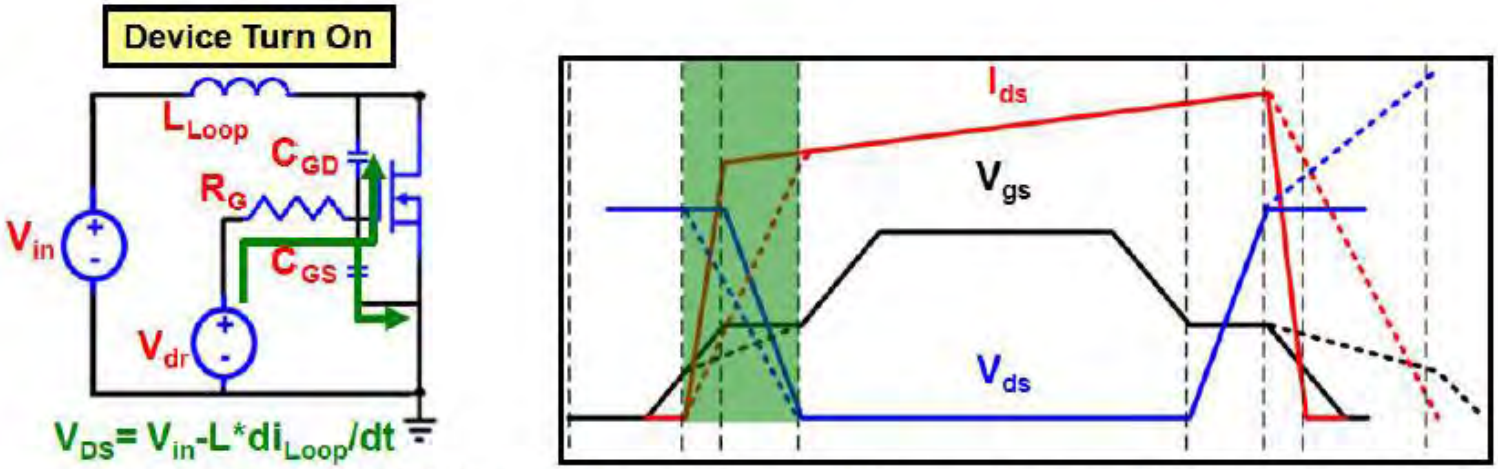
L_S: Common Source Inductance

L_{Loop}: High Frequency Power Loop Inductance

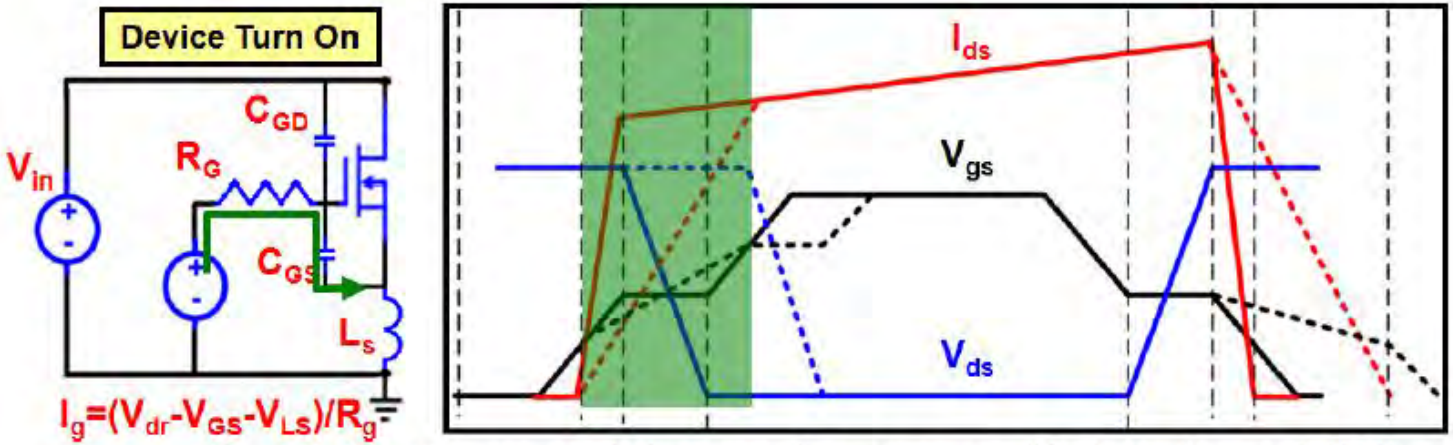


V_{IN}=12 V, V_{OUT}=1.2 V,
F_S=1 MHz, I_{OUT}= 20 A

Lloop & CSI impact on *turn on*

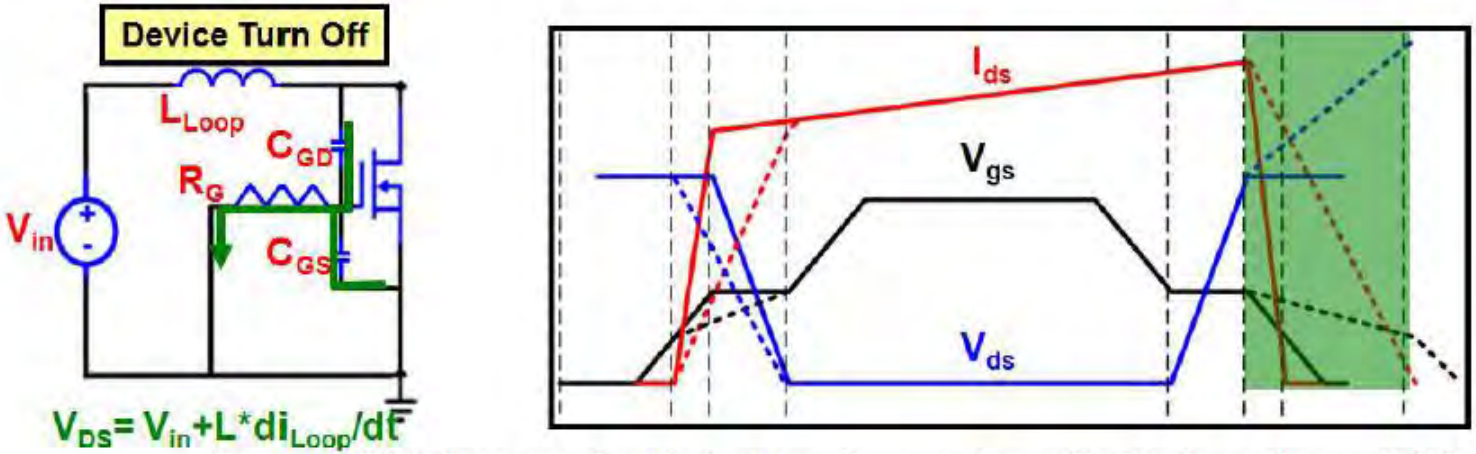


Impact of high frequency loop inductance, L_{Loop}, on turn on. Ideal waveforms: Solid line, Waveforms with parasitic influence: Dashed line



Impact of common source inductance, L_S, on turn on. Ideal waveforms: Solid line, Waveforms with parasitic influence: Dashed line

Lloop & CSI impact on *turn off*



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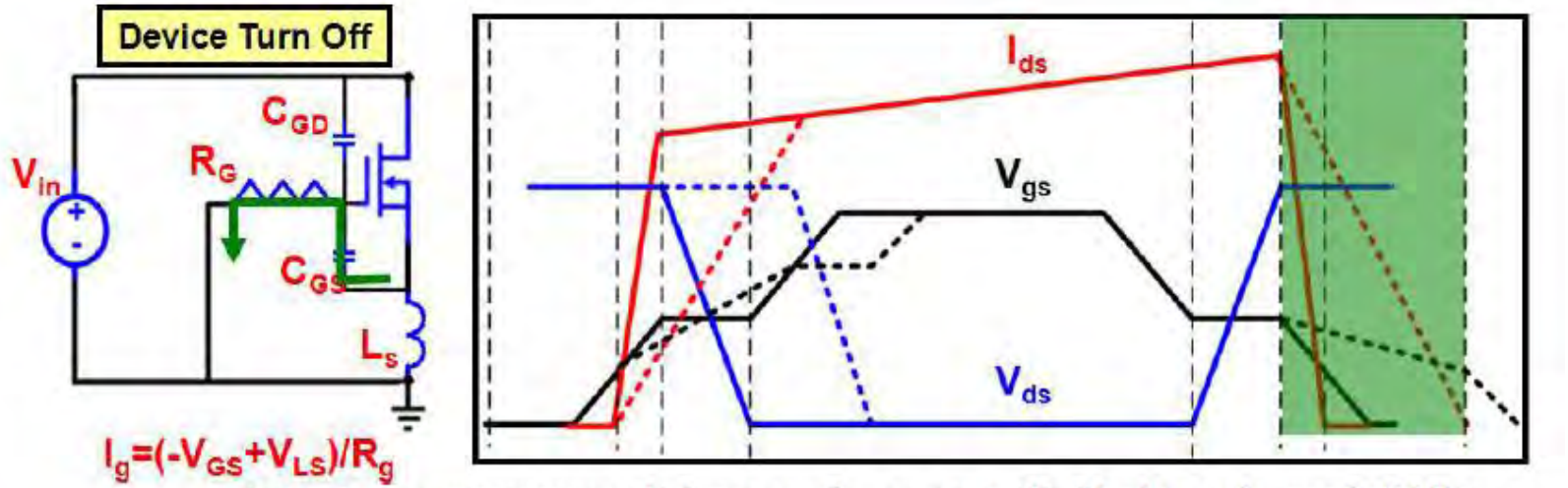
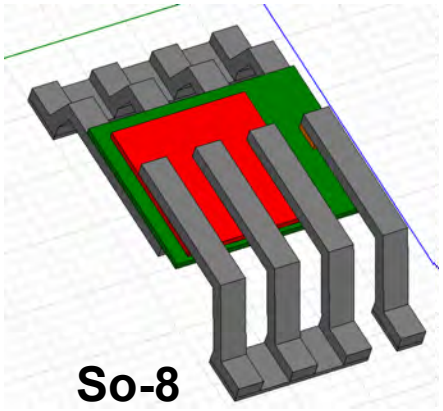
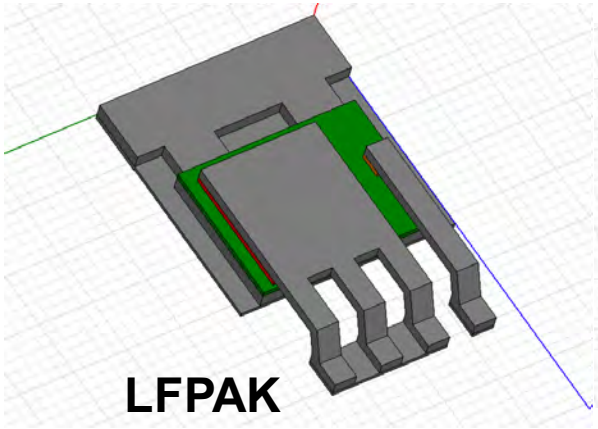
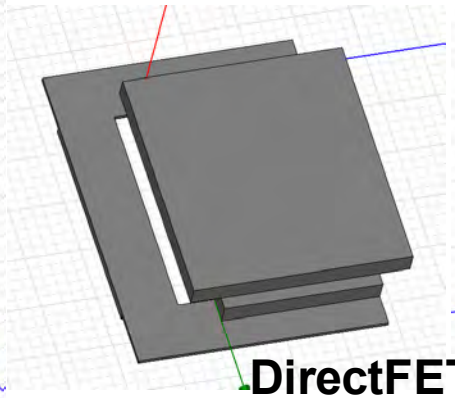


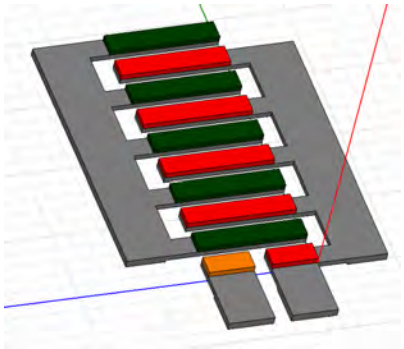
Impact of common source inductance, L_S, on turn off. Ideal waveforms: Solid line, Waveforms with parasitic influence: Dashed line

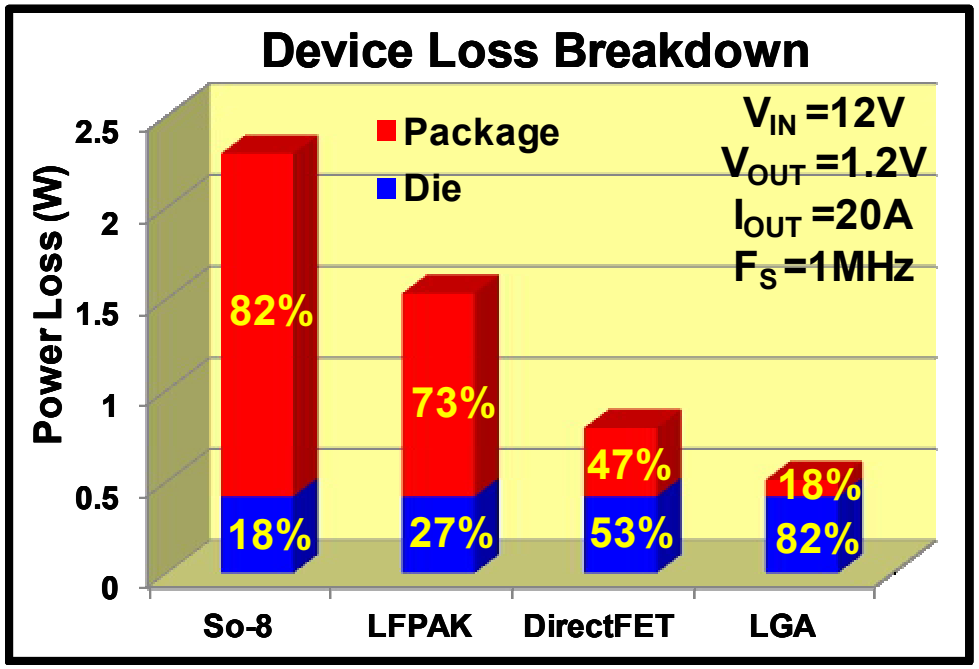
Packaging Evolution

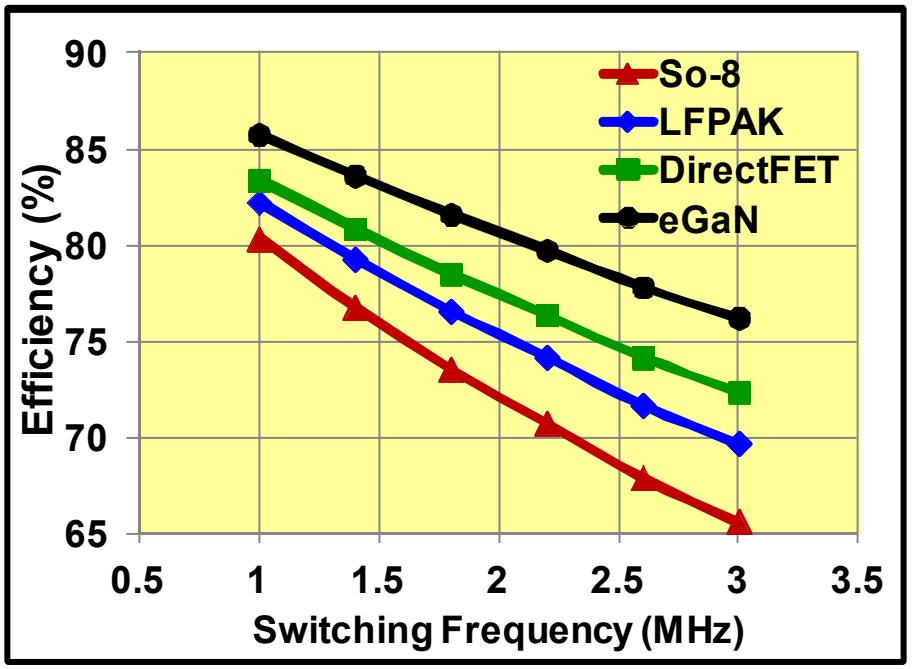






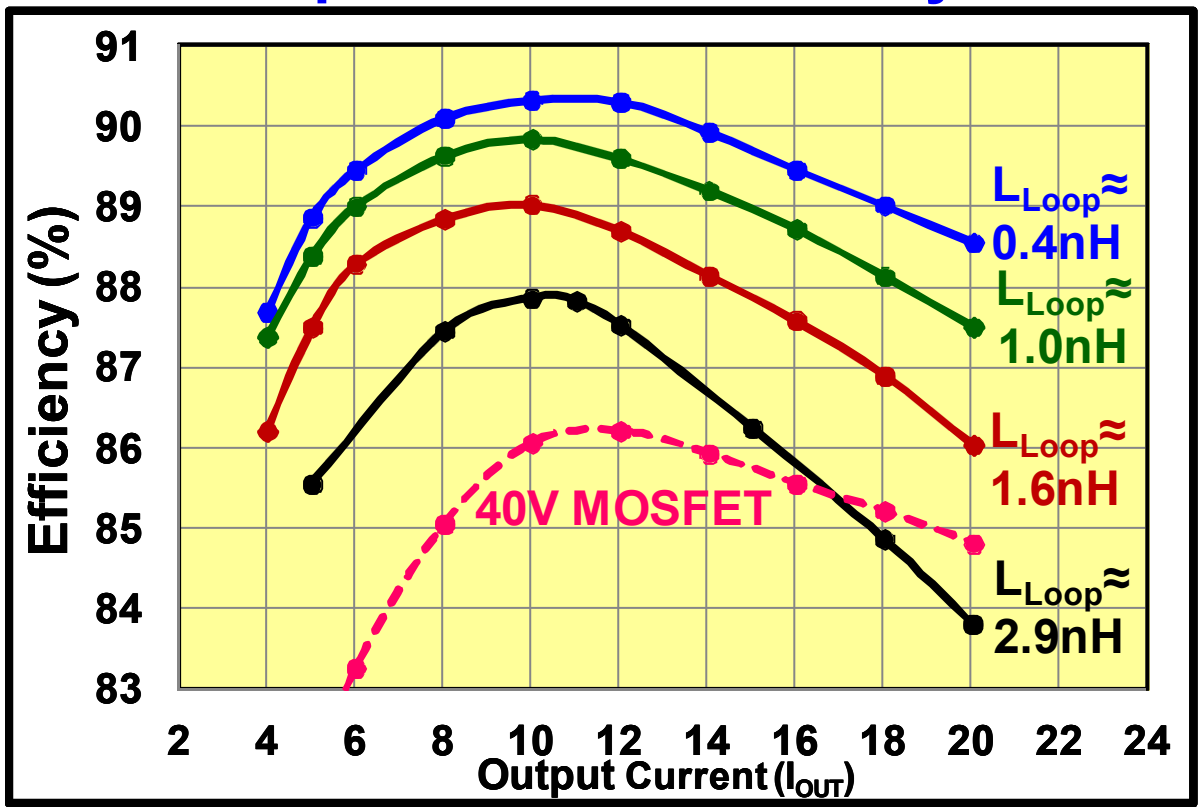






Layout Impact on Efficiency

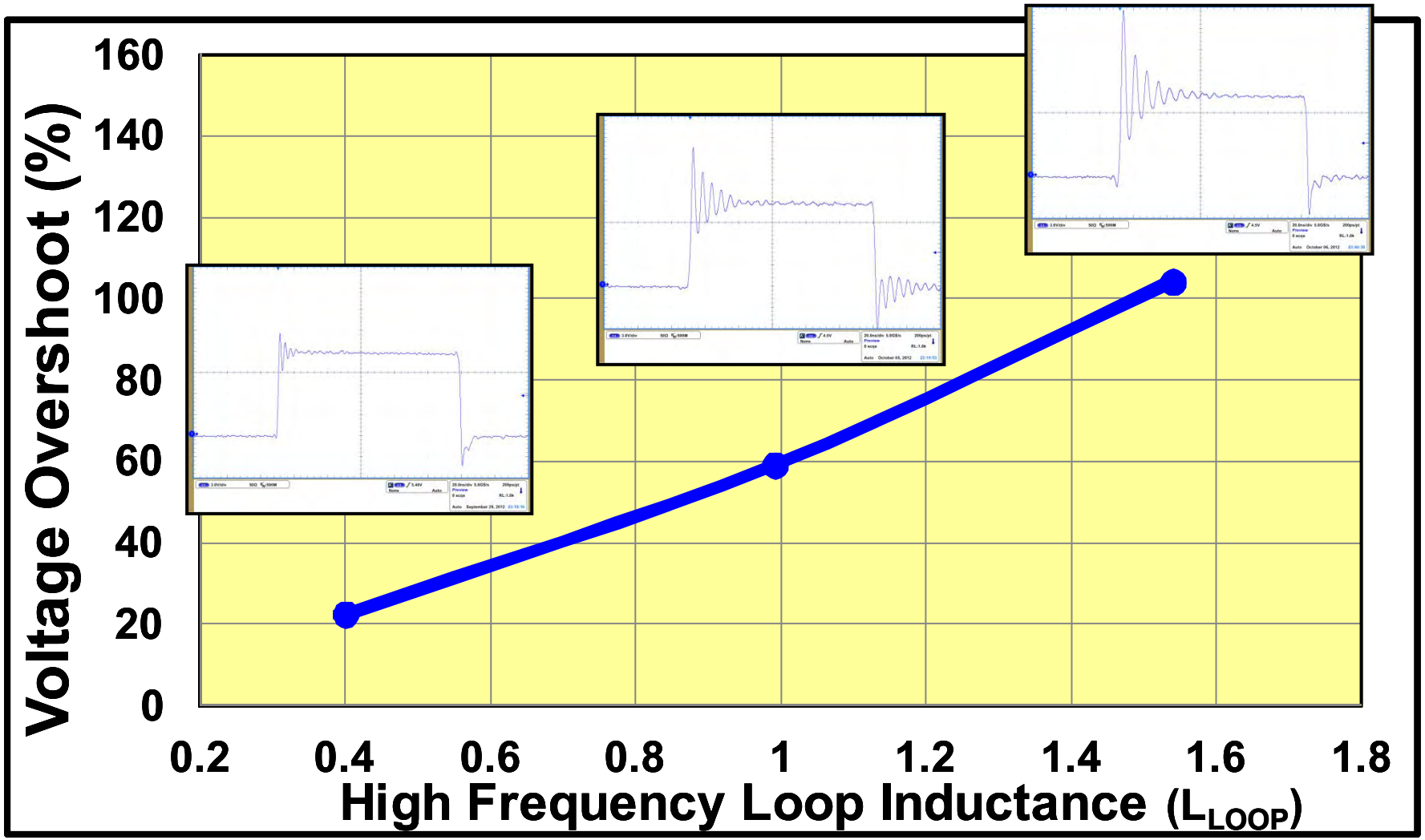
Experimental Efficiency



Optimal Layout Prototype

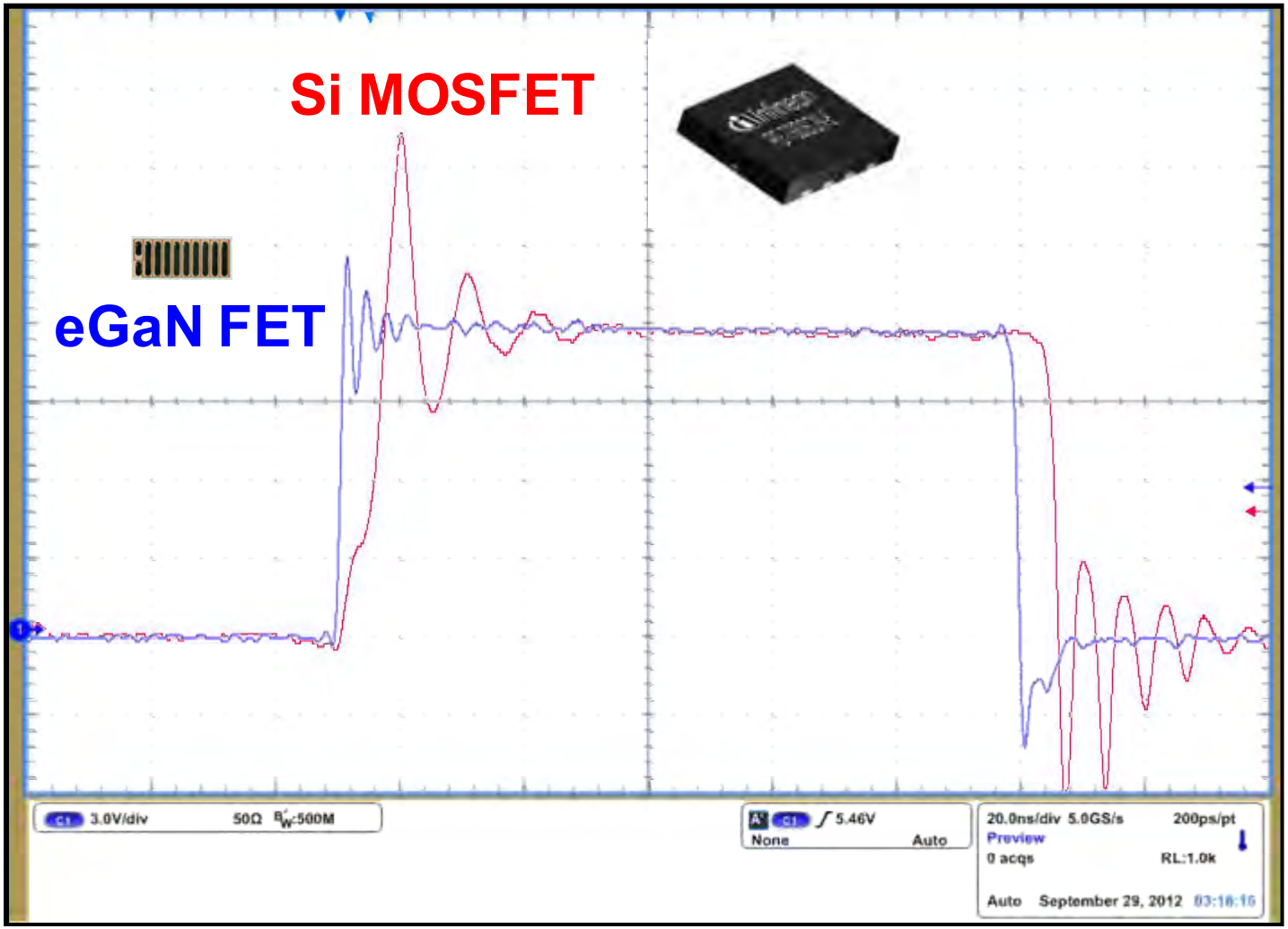
V_{IN}=12 V, V_{OUT}=1.2 V,
F_S=1 MHz, L=150 nH

Peak Voltage Comparison



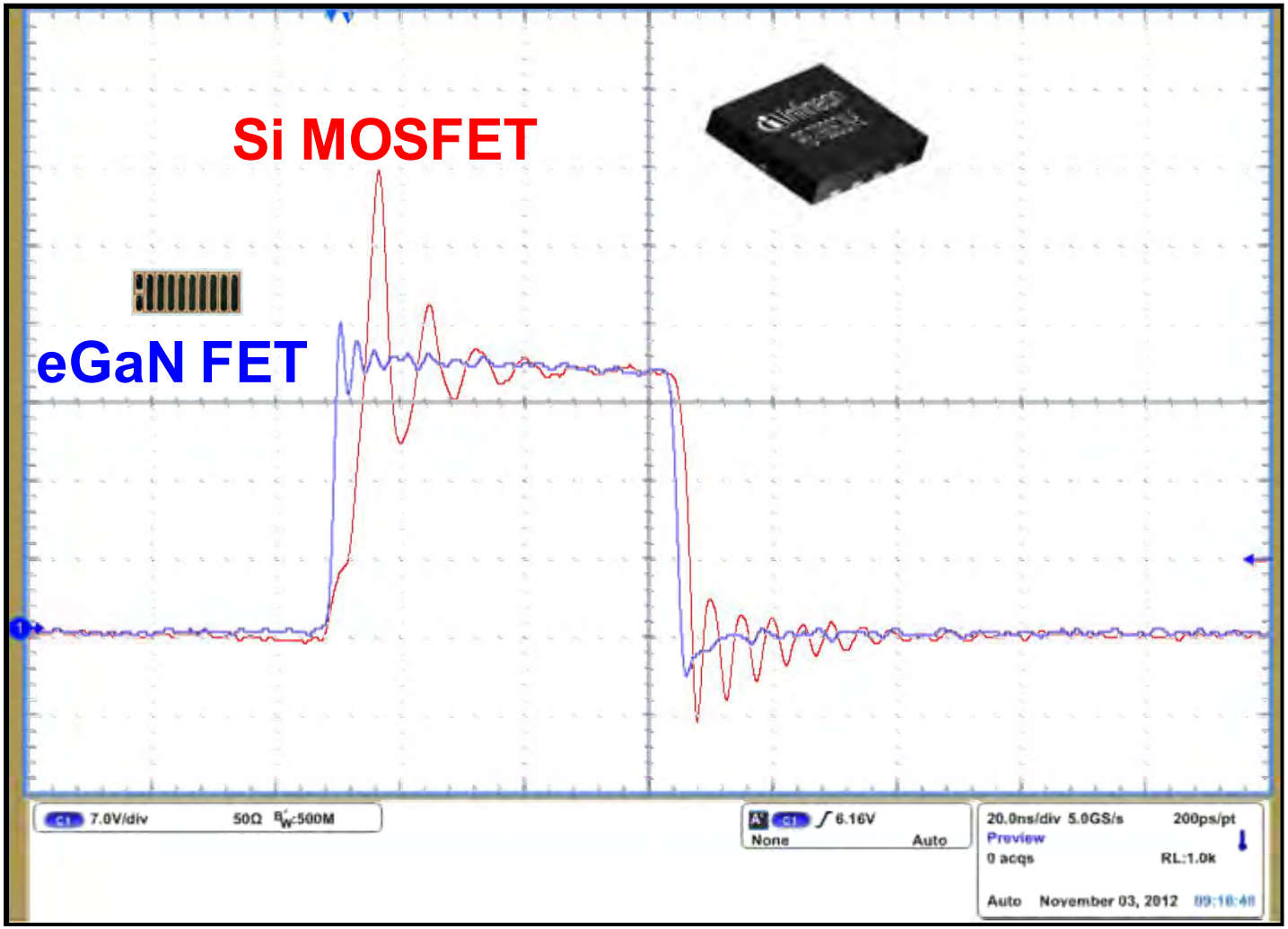
V_{IN}=12 V, V_{OUT}=1.2 V, F_S=1 MHz, L=150 nH

Experimental Waveforms



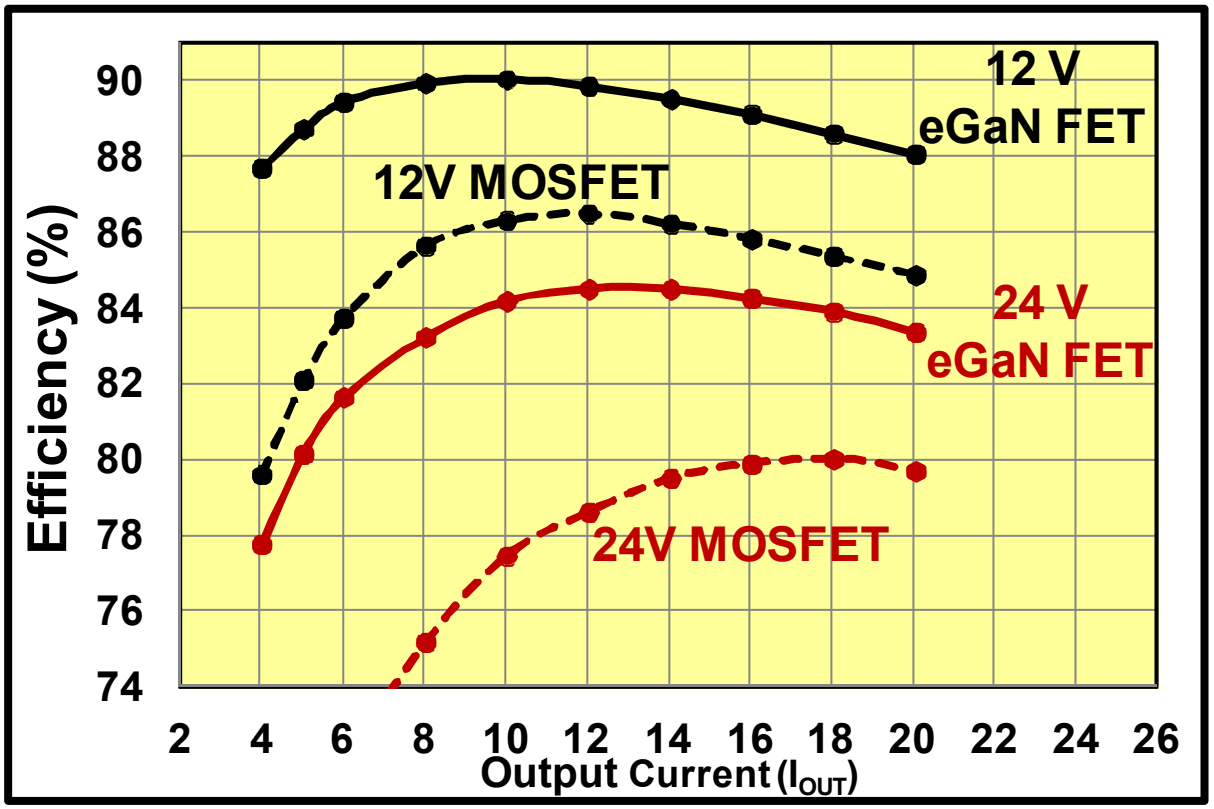
V_{IN}=12 V, V_{OUT}=1.2 V, F_S=1 MHz, L=300 nH

Experimental Waveforms



V_{IN}=24 V, V_{OUT}=1.2 V, F_S=1 MHz, L=300 nH

Optimal Layout Efficiency

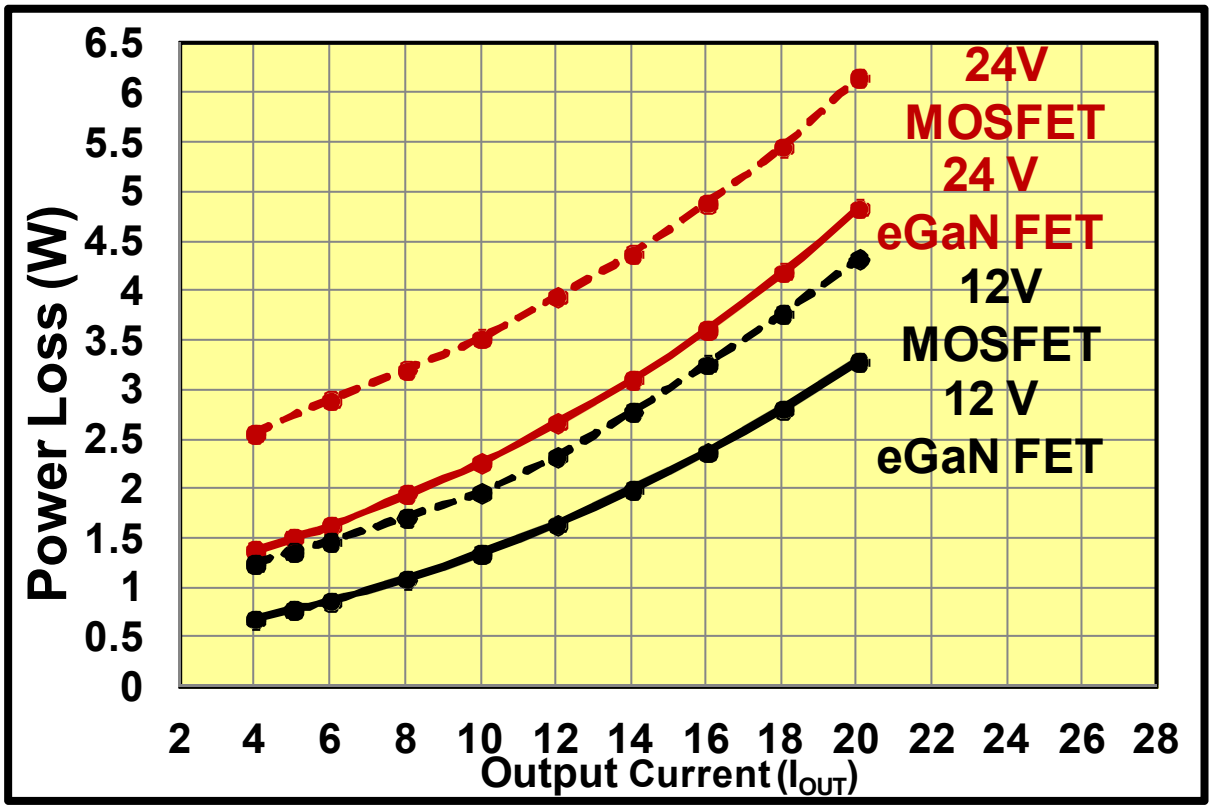


V_{OUT}=1.2 V, F_S=1 MHz, L=300 nH

eGaN FET: Top: EPC2015 SR: EPC2015

Si MOSFET: Top: BSZ097N04 SR: BSZ04N04

Optimal Layout Power Loss



V_{OUT}=1.2 V, F_S=1 MHz, L=300 nH

eGaN FET: Top: EPC2015 SR: EPC2015

Si MOSFET: Top: BSZ097N04 SR: BSZ04N04

Summary

eGaN FETs can improve high frequency hard switching converter performance:

- **Lower Switching Charge (Q_{GD}+Q_{GS2})**
- **Lower Gate Charge (Q_G)**
- **Improved Packaging**
- **Improved Layout Capability**

What Other Advances are Needed?

- High speed digital controller ICs and integrated controller/driver ICs.
  - Application specific controllers to reduce time-to-market
  - Dynamic deadtime control with ~1ns resolution
  - Synchronous PFCs
  - Envelope Tracking Controllers
- Note: Improvements in magnetics would be helpful…

EPC
EFFICIENT POWER CONVERSION

The end of the road for silicon…..

is the beginning of the eGaN FET journey!